

FORM PTO-1449 (Modified for Citation of Foreign
Cited References)ATTY. DOCKET NO.
USA.02.022SERIAL NO.
10/091086LIST OF INFORMATION PROVIDED
BY APPLICANT

APR 15 2002

(Use several sheets if necessary)

APPLICANT
STEWART, et alFILING DATE
March 5, 2002GROUP
Unknown

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date*	Patentee	Date* Cited in Foreign Patent Office
TT	AA	5,930,889	8/3/1999	Klein	
TT	AB	6084781	7/4/2000	Klein	
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TT	AD	5061549	10/29/1991	Shores	
TT	AE	5372883	12/13/1994	Shores	
TT	AF	6297560	10/02/2001	Capote et al	
TT	AG	6265776	7/24/2001	Gilleo	

FOREIGN PATENT DOCUMENTS

		Document No.	Country	Date*	Date* Cited in Foreign P.O.	English Translation	
						Yes	No
	FA						
	FB						

OTHER PUBLICATIONS (AUTHOR, TITLE, DATE*, PLACE OF PUBLICATION, PERTINENT PAGES)

			Date* Cited in Foreign P.O.	English Translation	
				Yes	No
TT	PA	Adamson, S.J., "CSP and flip chip underfill," Advanced Packaging, June 2001, pp. 37-44.			
TT	PB	Johnson, Zane, "BGA Underfills" Advanced Packaging, December 2001, pp. 29-33.			
TT	PC	Alpha Microelectronic: Staystik Adhesive for Mag Heads, [internet] Retrieved on December 19, 2001, URL: www.us-tech.com/april99/prods/cmp/cmp016.htm			
TT	PD	Center for Advanced Vehicle Electronics, "Ball Grid Array Reliability" [Internet] Retrieved on January 8, 2002, URL: www.eng.auburn.edu/departement/ee/cave/bgareliability.html			
TT	PE	Brofman, P.J., "Effect of Underfill Properties on Flip Chip Plastic BGA (FC-PBGA) Reliability," IPC, Session P-MT1/5-(1-5); Presented at Apex 2000, March 14-16, 2000; Long Beach Convention Center, Long Beach, CA			

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Thien K. M.

DATE CONSIDERED

04/08/04

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TT	AH	5783867	7/21/1998	Belke, et al	
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OTHER PUBLICATIONS (AUTHOR, TITLE, DATE*, PLACE OF PUBLICATION, PERTINENT PAGES)

			Date* Cited in Foreign P.O.	English Translation	
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TT	PF	Adamson, Steven J, "When to Underfill Chip Scale Packages, Design Consideration for Portable Electronic Applications," IPC, Session P-AD2/2-(1-8); Presented at Apex 2000, March 14-16, Long Beach Convention Center			
TT	PG	Ghaffarian, R., "Impact of CSP Assembly Underfill Reliability," IPC, Session P-AD2/3-(1-7); Presented at Apex 2000, March 14-16, Long Beach Convention Center			
TT	PH	Yaeger, E., "Beyond Flip-Chip, Underfills Enhance CSP Reliability," Chip Scale Review, March 2001, pp. 61-66			
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TT	PK	Hannan, N., "Critical Aspects of Reworkable Underfills for Portable Consumer Products," 2001 Electronic Components and Technology Conference, 2001 IEEE, pp 181-187			
TT	PL	Chapter C: Conductive Polymers, Level 1: Introduction [internet], last updated on 2000-09-07; URL: http://extra.ivf.se/ngl/C-polymerBonding/ChapterC.htm			
TT	PM	Kristiansen, H., "Adhesives in Electronics," Chalmers Tekniska Hogskola, SINTEF Microelectronics; Presented at International Microelectronics and Packaging Society, Flipchip Technology Workshop, June 18-20, 2001			
TT	PN	Tong, Q., "Novel Fast Cure and Reworkable Underfill Materials," 1999 Electronic Components and Technology Conference, 0-7803-5234-3/99, 1999 IEEE, pp.			

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DATE CONSIDERED 07/08/04

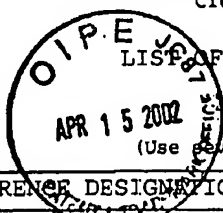
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	APPLICANT STEWART, et al	
	FILING DATE March 5, 2002	GROUP Unknown



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TT	PO	Nguyen, L., "Reworkable Flip Chip Underfill-Materials and Processes," Proc. IMAPS International Symposium on Microelectronics, pp. 707-713 (1998).			
TT	PP	Gilleo, K., "The Great Underfill Race," [internet] URL: http://www.cooksonsemi.com/tech_art/polysolder.htm			
TT	PQ	Gilleo, K., "Wafer-Level Flux Underfill: Underflip," Presented at Apex 2000, March 14-16, 2000; Long Beach Convention Center; Session P-MT1/4-(1-5)			
TT	PR	Thorpe, R., "Low Cost Flip Chip Processing Utilizing No Flow Underfill Materials," Presented at Apex 2000, March 14-16, 2000; Long Beach Convention Center; Session P-AP3/3-(1-8)			
TT	PS	Hackett, S., "A No-flow Underfill With Excellent Reliability Performance," IMAPS Flip Chip 2001 Austin, Texas June 18 - 19, 2001			
TT	PT	Suzuki, O., "Research on the Development of Advanced Non Conductive Paste (ANCP), Imaps Conference on Flip Chip Technology in Austin, Texas; June 18-19, 2001			
TT	PU	PRC Research Project Summaries, Flip Chip Assembly Thrust, [internet] Obtained October 31, 2001, URL: www.ee.gatech.edu/research/PRC/research/projsummary/asm.htm			
TT	PV	Emerson, J., "Techniques for Determining the Flow Properties of Underfill Materials," 1999 electronic Components and Technology Conference, 0-7803-5234-3/99			
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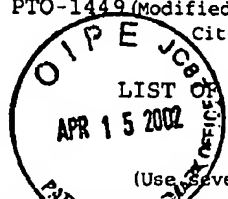
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TT	PZ	Goyal, S, "Role of Shock Response Spectrum in Electronic Product Suspension Design," The International Journal of Microcircuits and Electronic Packaging, Volume 23, Number 2, Second Quarter 2000, pp 182-190			
TT	PAA	Yamaji, Y., "A proposal: the Assessing Method of the CSP's Mechanical Reliability on Board," The International Journal of Microcircuits and Electronic Packaging, Volume 23, Number 1, First Quarter 2000, pp 138-145			
TT	PBB	Goyal, S, "Methods for Realistic Drop-Testing," The International Journal of Microcircuits and Electronic Packaging, Volume 23, Number 1, First Quarter 2000, pp. 45-52			
TT	PCC	Xu, K., "A General Purpose Adhesive for Microelectronic Devices," The International Journal of Microcircuits and Electronic Packaging, Volume 23, Number 1, First Quarter 2000, pp. 78-84			
TT	PDD	Seppala, A, "Flip Chip Joining on GR-4 Substrate Using ACFs," The International Journal of Microcircuits and Electronic Packaging, Volume 24, Number 2, Second Quarter 2001, pp. 148-159			
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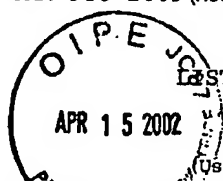
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			Date* Cited in Foreign P.O.	English Translation	
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TT	PEE	Gilleo, K., "New Generation Underfills Power The 2 nd Flip Chip Revolution," [internet] URL: http://www.cooksonsemi.com/tech_art/polysolder.htm			
TT	PFF	Hung, S.C., "Board Level Reliability of Chip Scale Packages," The International Journal of Microcircuits and Electronic Packaging, Volume 23, Number 1, First Quarter 2000, pp. 118-130			
TT	PGG	Gilleo, K., "Transforming Flip Chip into CSP with Reworkable Wafer-Level Underfill," [internet] URL: http://www.cooksonsemi.com/tech_art/staychip.htm			
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TT	PJJ	Gilleo, K., "The Chemistry & Physics of Underfill," [internet] URL: http://www.cooksonsemi.com/tech_art/staychip.htm			
TT	PKK	Harper, P., "Thermoplastic Die Attach For Hermetic Packaging," The International Journal of Microelectronics and Electronic Packaging, Vol. 17, No. 4, Fourth Quarter, 1994, pp			
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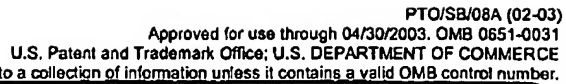
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Substitute for form 1448/PTO

(Use as many sheets as necessary)

Complete if Known

Application Number	10/091, 086
Filing Date	03/05/2002
First Named Inventor	Stewart, Steven L.
Art Unit	
Examiner Name	
Attorney Docket Number	US.01.012

Sheet	1	of	2
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U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (# known)	MM-DD-YYYY			
TT		EP 0729182A	08-28-1996	Matsushita Electric Inc		
TT		DE 19822470A	12-09-1999	Litton Precision Product		
TT		JP 08250835A	09-27-1996	NEC Corp		
TT		JP 10335527A	12-18-1998	NEC Corp		
TT		JP 03036788A	02-18-1991	Murata Mfg Co Ltd		
TT		JP 04249307A	09-04-1992	Nippon Chemicon Corp		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	2
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Complete if Known

Application Number	10/091,086
Filing Date	03/05/2002
First Named Inventor	Stewart, Steven L.
Art Unit	
Examiner Name	
Attorney Docket Number	US.01.012

U. S. PATENT DOCUMENTS

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		Country Code ³ *Number ⁴ *Kind Code ⁵ *(if known)	MM-DD-YYYY			
TI		JP 05347474 A	12-27-1993	Matsushita Electric Ind		
TI		JP 57068053 A	04-26-1982	Seiko Epson Corp		
TI		JP 04352491 A	12-7-1992	Matsushita Electric Ind		

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